

REMARKS

Applicant appreciates the time taken by the Examiner to review Applicant's present application. This application has been carefully reviewed in light of the Official Action mailed June 15, 2006. Applicant respectfully requests reconsideration and favorable action in this case.

DRAWINGS OBJECTIONS

The applicant respectfully submits that the enclosed replacement sheets are submitted to overcome the examiners objections.

SPECIFICATION OBJECTIONS

The applicant respectfully submits that paragraph [0026] has been amended to overcome the examiners objections.

CLAIM OBJECTIONS

Claims 1,12,13, and 32 are objected to because of informalities. The applicant respectfully submits that Claims 1, 12, 13 and 32 have been amended to overcome these informalities.

CLAIM REJECTIONS - 35 USC §112

Claims 11, 13, 16, 23, 24, 29, and 34 are rejected under 35 U.S.C. 112, second Paragraph, as being indefinite for failing to particularly point out and distinctiy Claim the subject matter which applicant regards as the invention. The examiner states:

Claims 11 and 23 recite the limitation "the battery reserve" in lines 6, respectfully. There is insufficient antecedent basis for this limitation in the Claim.

Claim 13, lines 12-13 recite the limitation "a battery". It is unclear if this is the same battery as disclosed in Claim 13, line 7.

Also, Claim 13, lines 13-14 recite the limitation "a crystal oscillator". It is unclear if this is the same crystal oscillator as disclosed in Claim 13, line 4.

Claim 16, line 3 recites the limitation "an on-chip DC-to-DC Converter". It is unclear if this Converter is the same as the DC-to-DC Converter as disclosed in Claim 13, line 5.

Claim 24, line 5 recites the limitation "a digital processing integrated circuit". It is unclear if this circuit is the same as the digital processing integrated circuit as disclosed in Claim 24, line 2.

Claim 29 recites the limitation "the plurality of persistent registers" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 34, lines 3-4 recite the limitation "an alarm dock setting". It is unclear if this setting is the same as the alarm dock setting disclosed in Claim 33, line 3.

The applicant respectfully submits that claims 11, 13, 16, 23, 24, 29, and 34 rejected under 35 USC § 112 have been amended to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Therefore, the applicant respectfully requests that the examiner withdraw the rejection to the claims 11, 13, 16, 23, 24, 29, and 34 rejected under 35 USC § 112.

CLAIM REJECTIONS - 35 USC § 103

Claims 1 - 7, 12 - 19, 24, 27 - 31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Korff (U.S. Patent No. 4,573,127), and further in view of Cox (U.S. Patent No. 5,778,239), and Blau, Jr. et al. (U.S. Patent No. 4,522,333). The examiner states:

As per Claim 24, Korff teaches a digital processing circuit (*Fig. 1 - microprocessor, 20; and col. 4, lines 9-10*) comprising:

an on-chip real time dock module whose Contents are periodically updated (*col. 4, lines 17-18*), wherein the Contents are timing Parameters (*col. 4, lines 48-61*);

a processor (*Fig. 1 - CPU, 22*) that periodically Updates the Contents of the real time dock module (*col. 4, lines 48-50 and 61-64*).

Korff does not specifically teach that the Contents of the real time dock module are operational parameters being managed, and wherein the real time dock module is powered by a power source and receives a dock signal from a crystal oscillator that remain active when the digital processing System is powered down. Korff also does not teach that the real time dock module provides the digital processing integrated circuit with the parameters when parameters of the integrated circuit are "stale". Specifically, Korff teaches a real time dock module whose contents are periodically updated. Korff fails specifically to teach that the stored contents are operational parameters, management of the parameters when they are found to be stale, and the power and signal sources for the real time dock module

Cox teaches a real time dock module (*Fig. 1*), wherein operational ("setup") parameters are stored in the real time dock module (*col. 2, lines 16-19*).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Korff and Cox because they both teach a real time dock module capable of storing contents. Cox's teaching of System parameters stored in the real time dock module shows the type of contents that may be stored in a real time dock module.

Blau, Jr. et al. (hereinafter, referred to as "Blau") teach a circuit comprising a real time dock module, wherein a crystal oscillator maintains a dock signal to the real time dock module and a battery maintains power supplied to the real time dock module when a power failure occurs (*col. 4, lines 67-68, col. 5, lines 1-7 and; Fig. 2*).

Blau also discloses that the battery allows the processor to resume Operation when main power is reestablished using retained information stored before a power-off (*col. 5, lines 2-7*).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Korff and Blau because they both teach a real time dock module, both inherently needing a power source and dock Signal to operate. Blau's teaching of the disclosed crystal oscillator and battery show that the real time dock module can maintain its functionality when power to the System is not available. In reference to the applicant's claimed method, it would have obvious that Blau's teachings can be applied to a real time dock module located on an integrated circuit, wherein power and a crystal oscillator signal are maintained at the real time dock module when power is not being supplied to the rest of the integrated circuit. Inherently, the contents ("information") stored in the real time dock module would be provided to the processor or the digital processing integrated Chip comprising the real time dock module. During a power-off State, information contents stored in the digital processing integrated circuit are inherently "stale" compared to the retained information backed up in the storage of the real time dock module, thus it would be required that the real time dock module provide the retained information content to the digital processing integrated circuit after the integrated circuit has resumed power-on. It is also well known in the art that audio processing chips may contain a digital processing integrated circuit comprising a real time dock module

As per Claim 27, Cox teaches a method of monitoring battery power levels (*col. 2, lines 32-42*). It is well known in the art that a digital processing integrated circuit would power down when battery levels go below a predetermined threshold and that current parameters would be stored prior to the power down, wherein the parameters could be stored on the real time dock module.

As per Claim 28, since Blau teaches that the crystal oscillator only maintains a dock signal to the real time dock module (*Fig. 2 and; col. 4, lines 67-68*), the rest of the digital processing integrated circuit would inherently operate on another dock domain, or the System dock domain.

As per Claim 29, it is well known in the art that when two dock domains are being used within an integrated circuit, wherein communication occurs between the

two domains (in this instance, between the digital processing integrated circuit and the real time dock module), it would have been obvious to use a module/circuit to synchronize the two domains so that data can be synchronously transferred between the two domains.

As per Claim 30, since the digital processing integrated circuit comprises two dock domains, it would have been obvious to one of ordinary skill in the art to use input/output buffers to temporarily store the parameters that are transferred from one dock domain to another since buffers are used to compensate for differences in operating speeds.

As per Claim 31, as mentioned above, Blau teaches that the real time dock module maintains a powered State when the rest of the System is powered down (*col. 4, lines 67-68, col. 5, lines 1-7*).

As per Claims 1, 3, 5, 6, 7, 12 it is directed to an apparatus of the on-chip real time dock module/digital processing integrated circuit method as set forth in Claims 24 and 27 - 31 above. Since Korff-Cox-Blau teach the claimed method of managing Parameters of a digital processing integrated circuit comprising an on-chip real time dock module, Korff-Cox-Blau also teach the apparatus having a digital processing integrated circuit and real time dock module.

As per Claim 2, since the digital processing integrated circuit operates on a different dock domain than of the on-chip real time dock module, and since parameters are transferred between the two domains, an interface is inherently required between the real time.

As per Claim 4, it would have been obvious to one of ordinary skill in the art that an on-chip DC-to-DC Converter powers the digital processing integrated circuit since, typically, integrated circuits use DC-to-DC Converters with the circuit comprises a battery.

As per Claims 13-19, Korff-Cox-Blau teach the claimed digital processing integrated circuit as applied to Claims 1 - 7 above.

Claims 8 - 11, 20 - 23, 25, 26, 32 - 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Korff, Cox, and Blau, Jr. et al. as applied to Claim 24 above, and further in view of Cornish et al. (U.S. Patent No. 5,943,507).

As per Claim 25, Korff-Cox-Blau teach the method of Claim 24 as mentioned above, however they do not teach that the digital processing integrated circuit comprises shadow registers to store the parameters. Specifically, Korff-Cox-Blau teach that the parameters are stored in an on-chip real time dock module and are provided to the digital processing integrated circuit. Korff-Cox-Blau fail to teach where the parameters are stored within the digital processing integrated circuit.

Cornish et al. (hereinafter, referred to as "Cornish") discloses a digital processing integrated circuit (*Fig. 11 - PPU 110 and; col. 15, lines 47-48*) comprising:

an on-chip real time dock module (*Fig. 11 - RTC, 918 and col. 16, lines 29-31*) and;

shadow registers (*col. 17, lines 18-19*).

It would have been obvious to one of ordinary skill in the art to combine the teachings of Korff-Cox-Blau and Cornish because they all teach the use of a real time dock module. Cornish's teaching of shadow registers comprised within the digital processing integrated circuit would allow a storage means for parameters temporarily stored in the real time dock module to be transferred to when power is restored in the digital processing integrated circuit.

As per Claim 26, it would have been obvious to one of ordinary skill in the art that the parameters contained within the shadow registers return to a default condition when the digital processing integrated circuit is powered down so that stale parameters can be detected after a power-down of the digital processing integrated circuit.

As per Claim 32, after parameters return to a default condition in response to a power-down of the digital processing integrated circuit, it is inherent that those

parameters stored in the integrated circuit are stale from that point on, including at a State of power-up since the parameters cannot be updated while power is not being supplied to the integrated circuit in a powered-down State.

As per Claims 33 and 34, to power up the digital processing integrated circuit, inherently, an interrupt Signal would need to be issued to the digital processing integrated circuit. It is known in the art that powering up a circuit may require a method of issuing a power-on interrupt/signal to the circuit in response to an alarm dock setting.

The real time dock module provides the digital processing integrated circuit with current parameters when parameters of the digital processing integrated circuit are found to be stale, as applied to Claim 24 above. The parameters are found to be stale at a State of power-up, as applied to Claim 32 above, thus, the real time dock module would supply current parameters to the digital processing integrated circuit at power up.

As per Claims 8 - 11, it is directed to an apparatus of the on-chip real time dock module/digital processing integrated circuit method as set forth in Claims 25, 26, 32 - 34 above. Since Korff-Cox-Blau teach the claimed method of managing parameters of a digital processing integrated circuit comprising an on-chip real time dock module, Korff-Cox-Blau also teach the apparatus having a digital processing integrated circuit and real time dock module.

As per Claims 20 - 23, Korff-Cox-Blau teach the claimed digital processing integrated circuit as applied to Claims 8-11 above.

The applicant respectfully submits that the operating parameters and timing parameters stored in the persistent registers of the present invention may be distinguished from the setup parameters of Cox. Cox provides setup parameters that may be stored in memory such as keyword, password, hard drive identification or ID numbers and the like. These setup parameters are required every time the computer described in Cox starts up. The operating parameters and timing parameters provided in the present invention are periodically stored in persistent registers. These operating parameters and timing parameters allow a device to power up in a known manner. In

particular, they allow the device to resume where the device left off just before the device powered down. This is different from the set up parameters of Cox which always start the computer in a known starting condition while the operating and timing parameters that are periodically stored to the persistent registers allow the digital processing integrated circuit to be restored to the state it was operating in prior to shut down. At no point does Cox periodically store operating and timing parameters as is done in the present invention as claimed when the input buffer periodically receives operational parameters and timing parameters from the digital processing integrated circuit periodically as directed for example by the controller of claim 3. The persistent registers may be updated at a pre-determined frequency or after pre-determined events occur. The setup parameters of Cox may be stored once.

With respect to Korff the applicant respectfully submits that Korff fails to teach that a timing module as directed to loading calendar events. Korff teaches the use of a calendar and fails to teach the storage of operations parameters associated with the operational state of a digital circuit, timing parameters associated with the operation of a digital circuit and the periodic storage of these parameters for use after the device is in a powered down condition. The applicant respectfully submits with respect to Blau that Blau teaches that a battery is used to provide power to a crystal oscillator in order to maintain a clock signal in the event of a power failure. Blau fails to teach the use of persistent registers for the storage of operating parameters associated with the circuit. Blau merely teaches that the real time clock signal is preserved. In fact, while Blau teaches that the battery merely provides a power backup in the event of a power failure Blau at no point teaches the storage of operating parameters in persistent registers.

The applicant therefore submits that one would not reach the claimed invention from the teachings of Korff and Balu and Cox.

Applicant respectfully points out that in order to combine references for an obviousness rejection, there must be some teaching, suggestion or incentives supporting the combination. *In re Laskowski*, 871 F.2d 115, 117, 10 U.S.P.Q. 2d 1397, 1399 (Fed. Cir. 1989). The mere fact that the prior art could be modified does not make that modification obvious unless the prior art suggests the desirability of the modification. *In re Gordon*, 733 F.2d 900, 902, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984). In addition, it is well established that Applicant's disclosure cannot be used to

reconstruct Applicant's invention from individual pieces found in separate, isolated references. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596 (Fed. Cir. 1988).


Applicant respectfully submits that there is no motivation, teaching or suggestion to combine Korff and Balu and Cox.. Therefore, the rejection on a combination of these references is inappropriate. Withdrawal of the rejection and allowance of Claims 1 - 7, 12 - 19, 24, 27 - 31 is respectfully requested.

CONCLUSION

Applicant has now made an earnest attempt to place this case in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicant respectfully requests full allowance of Claims 1-34.

An extension of three (3) months is requested under 37 C.F.R. § 1.136 with the appropriate fee attached. While Applicants believe no fee is due with this transmission, if any fees are due, the Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 50-2126 of Garlick Harrison & Markison, LLP.

Respectfully submitted,



By: _____

Robert A. McLauchlan
Reg. No. 44,924

ATTORNEY FOR APPLICANT

Dated: December 11, 2006

Garlick, Harrison & Markison, LLP

P.O. Box 26780

Austin, Texas 78755

(512) 339-4100

(512) 692-2529 (Fax)